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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,207	01/20/2004	Darin Chan	50432-470	8068

7590 02/22/2005

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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,207	CHAN ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/20/04 & 4/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communication filed January 20, 2004.

Information Disclosure Statement

The IDS filed on January 20, 2004 has been considered. The IDS filed on April 27, 2004 lists only one reference (US 5,970,362). This reference is already listed on the IDS filed 1/20/2004; therefore, a line has been drawn through this reference on the 4/27/04 IDS.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the specification fails to provide antecedent basis for the limitation in claim 15 of "etching under reflux boiling of phosphoric acid at about 180°C".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-11, 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Yuzuriha (US 6,682,985).

Regarding claim 1, Yuzuriha discloses forming a pad oxide layer (2) on a main surface of a substrate (1), forming a polish stop layer (4) on the pad oxide layer, forming an opening in the polish stop layer, pad oxide layer and an opening extending into the substrate, filling the opening in the substrate with a dielectric material (8) forming an overburden on the polish stop layer, planarizing the overburden, etching to remove a portion of the dielectric material forming a step between the dielectric material and the polish stop layer, and removing the polish stop layer (Fig. 1-4, 8-10; col. 10, ln. 45 – col. 11, ln. 22; col. 12, ln. 7 – col. 13, ln. 11).

Regarding claim 3, Yuzuriha discloses that the polish stop layer is silicon nitride (col. 10, ln. 49).

Regarding claim 4, Yuzuriha discloses that the dielectric layer is silicon oxide (col. 10, ln. 62-64).

Regarding claim 5, Yuzuriha discloses depositing the dielectric material by chemical vapor deposition on the polish stop layer filling the opening and forming the overburden (Fig. 4; col. 11, ln. 9-11).

Regarding claim 6, Yuzuriha discloses planarizing the overburden by chemical mechanical polishing such that an upper surface of the dielectric material is coplanar with an upper surface of the polish stop layer (Fig. 8; col. 12, ln. 10-16).

Regarding claims 7, 8, 13 and 14, Yuzuriha discloses etching to form the step of about 1000 Angstroms (col. 12, ln. 33-37).

Regarding claims 9 and 11, Yuzuriha discloses forming an oxide liner (7) in the opening in the substrate before filling the opening with dielectric material (col. 10, ln. 58-62).

Regarding claim 10, Yuzuriha discloses forming a pad oxide layer (2) on a semiconductor substrate (1), forming a silicon nitride polish stop layer (4) on the pad oxide layer, etching to form an opening in the polish stop and pad oxide layers, etching to form an opening extending into the substrate, depositing a layer of silicon oxide (8) on the polish stop layer filling the opening in the substrate, conducting chemical-mechanical polishing such that an upper surface of the silicon oxide layer is substantially coplanar with an upper surface of the polish stop layer, etching to reduce the upper surface of the silicon oxide layer so that it is below the upper surface of the polish stop layer, and removing the polish stop layer (Fig. 1-4, 8-10; col. 10, ln. 45 – col. 11, ln. 22; col. 12, ln. 7 – col. 13, ln. 11).

Claims 1-4, 6 and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimizu (US 6,846,721).

Regarding claim 1, Shimizu discloses forming a pad oxide layer (102) on a main surface of a substrate (101), forming a polish stop layer (103) on the pad oxide layer, forming an opening in the polish stop layer, pad oxide layer and an opening extending into the substrate, filling the opening in the substrate with a dielectric material (109) forming an overburden on the polish stop layer, planarizing the overburden, etching to remove a portion of the dielectric material forming a step between the dielectric material and the polish stop layer, and removing the polish stop layer (Fig. 1-8; col. 10, ln. 45 – col. 11, ln. 22; col. 12, ln. 7 – col. 13, ln. 11).

Regarding claims 2 and 12, Shimizu discloses depositing a gate layer (111) of polycrystalline silicon and etching/patterning it to form a gate electrode (col. 5, ln. 38-54).

Regarding claim 3, Shimizu discloses that the polish stop layer is silicon nitride (col. 3, ln. 55-57).

Regarding claim 4, Shimizu discloses that the dielectric layer is silicon oxide (col. 4, ln. 31-32).

Regarding claim 6, Shimizu discloses planarizing the overburden by chemical mechanical polishing such that an upper surface of the dielectric material is coplanar with an upper surface of the polish stop layer (Fig. 7; col. 4, ln. 38-40).

Regarding claims 9 and 11, Shimizu discloses forming an oxide liner (115) in the opening in the substrate before filling the opening with dielectric material (col. 4, ln. 20-25).

Regarding claim 10, Shimizu discloses forming a pad oxide (102) on a semiconductor substrate (101), forming a silicon nitride polish stop layer (103) on the pad oxide layer, etching to form an opening in the polish stop and pad oxide layers, etching to form an opening extending into the substrate, depositing a layer of silicon oxide (109) on the polish stop layer filling the opening in the substrate, conducting chemical-mechanical polishing such that an upper surface of the silicon oxide layer is substantially coplanar with an upper surface of the polish stop layer, etching to reduce the upper surface of the silicon oxide layer so that it is below the upper surface of the polish stop layer, and removing the polish stop layer (Fig. 1-8; col. 10, ln. 45 – col. 11, ln. 22; col. 12, ln. 7 – col. 13, ln. 11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuzuriha (US 6,682,985) in of the admitted prior art.

Regarding claims 2 and 12, Yuzuriha discloses forming semiconductor memory devices on the substrate, but does not specifically disclose depositing a gate layer of polycrystalline silicon and etching the layer to form a gate electrode. However, Applicant's specification admits that the steps of depositing a polysilicon gate layer and patterning it to form gate electrodes is conventional (pg. 5, ln. 12-13). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form a polysilicon gate on the substrate of Yuzuriha because Yuzuriha discloses forming semiconductor memory devices on the substrate and the admitted prior art states that these gate-forming steps are conventional.

Regarding claim 15, Yuzuriha discloses stripping the silicon nitride polish stop layer by using an etching liquid, but does not disclose any additional details of the stripping process. Applicant's specification admits that the stripping process used to remove the silicon nitride pad layer of their invention, is conventional (pg. 4, ln. 24-25). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the admitted prior art stripping process to remove the silicon nitride layer of Yuzuriha because Yuzuriha discloses using a liquid stripping process and because the admitted prior art states that this stripping process is conventional.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (US 6,846,721) in of the admitted prior art.

Regarding claim 15, Shimizu discloses stripping the silicon nitride polish stop layer by using hot phosphoric acid, but does not disclose any additional details of the stripping process.

Applicant's specification admits that the stripping process used to remove the silicon nitride pad layer of their invention, is conventional (pg. 4, ln. 24-25). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the admitted prior art stripping process to remove the silicon nitride layer of Shimizu because Shimizu discloses using a hot phosphoric acid stripping process and because the admitted prior art states that this stripping process is conventional.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
February 17, 2005

AMIR ZARABIAN
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